IN THE CLAIMS

1. (Currently Amended) A non-volatile semiconductor memory device having a memory cell array of aligning plural numbers of memory cells in a matrix-like manner, each of said memory cells comprising:

a source region formed in a semiconductor substrate;

a drain region formed in said semiconductor substrate;

a channel region formed between said source region and said drain region, and in said semiconductor substrate;

a gate electrode for controlling potential of said channel region; ~~and~~

plural numbers of charge storage grains formed between said gate electrode and said channel region, and isolated from said gate electrode and said channel region and with each other by an insulator~~, wherein~~ ;

a first charge storage region formed with a first set of said plural charge storage grains arranged in a vicinity of said source region; and

a second charge storage region formed with a second set of said plural charge storage grains arranged in a vicinity of said drain region, wherein,

a first memory cell and a second memory cell neighboring with each other in the direction of channel length share said source region in common;

each of said first charge storage region and said second charge storage region stores one bit of information, respectively; and

each of said memory cells stores two bits of information.

2. (Currently Amended) A non-volatile semiconductor memory device having a memory cell array of aligning plural numbers of memory cells in a matrix-like manner, each of said memory cells comprising:

a source region formed in a semiconductor substrate;

a drain region formed in said semiconductor substrate;

a channel region formed between said source region and said drain region, and in said semiconductor substrate;

a gate electrode for controlling potential of said channel region; ~~and~~

plural numbers of charge storage grains formed between said gate electrode and said channel region, and

isolated from said gate electrode and said channel region and with each other by an insulator~~, wherein~~;

first charge storage region formed with a first set of said plural charge storage grains arranged in a vicinity of said source region; and

second charge storage region formed with a second set of said plural charge storage grains arranged in a vicinity of said drain region, wherein

a first memory cell and a second memory cell neighboring with each other in the direction of channel length share said source region in common; ~~and~~

said second cell shares said drain region in common with a third memory cell neighboring in the direction of channel length therewith;

each of said first charge storage region and said second charge storage region stores one bit of information, respectively, and

each of said memory cells stores two bits of information.

3. (Currently Amended) A non-volatile semiconductor memory device having a memory cell array of aligning plural

numbers of memory cells in a matrix-like manner, each of said memory cells comprising:

a source region formed in a semiconductor substrate;

a drain region formed in said semiconductor substrate;

a channel region formed between said source region and said drain region, and in said semiconductor substrate;

a gate electrode for controlling potential of said channel region; ~~and~~

plural numbers of charge storage grains formed between said gate electrode and said channel region, and isolated from said gate electrode and said channel region and with each other by an insulator~~, wherein~~;

first charge storage region formed with a first set of said plural charge storage grains arranged in a vicinity of said source region; and

second charge storage region formed with a second set of said plural charge storage grains arranged in a vicinity of said drain region, wherein

plural numbers of cell separation regions in said memory cell array are aligning in parallel to each other, substantially;

plural numbers of word lines for connecting said gate electrodes of said memory cells are aligning in parallel to each other, substantially;

said memory cell shares a diffusion layer of said source region in common with only one memory cell neighboring in the direction of channel length therewith;

each source region of at least three of said memory cells neighboring in the direction of channel width are connected with one another through a metal wiring; ~~and~~

said cell separation region is perpendicular to said metal wiring, substantially, and said cell separation region is perpendicular to said word line, substantially;

each of said first charge storage region and said second charge storage region stores one bit of information, respectively; and

each of said memory cells stores two bits of information.

4. (Currently Amended) A non-volatile semiconductor memory device having a memory cell array of aligning plural numbers of memory cells in a matrix-like manner, each of said memory cells comprising:

a source region formed in a semiconductor substrate;

a drain region formed in said semiconductor substrate;

a channel region formed between said source region and said drain region, and in said semiconductor substrate;

a gate electrode for controlling potential of said channel region; ~~and~~

plural numbers of charge storage grains formed between said gate electrode and said channel region, and isolated from said gate electrode and said channel region and with each other by an insulator~~, wherein~~;

first charge storage region formed with a first set of said plural charge storage grains arranged in a vicinity of said source region; and

second charge storage region formed with a second set of said plural charge storage grains arranged in a vicinity of said drain region, wherein

plural numbers of cell separation regions in said memory cell array are in a rectangular shape, aligning in parallel to each other, substantially;

plural numbers of word lines for connecting said gate electrodes of said memory cells are aligning in parallel to each other, substantially;

plural numbers of said source regions thereof are connected with each other through a diffusion layer wiring;

plural numbers of diffusion layer wirings aligning in parallel to each other, substantially; ~~and~~

said cell separation region is perpendicular to said diffusion layer wiring, substantially, and said cell separation region is perpendicular to said word line, substantially;

each of said first charge storage region and said second charge storage region stores one bit of information, respectively; and

each of said memory cells stores two bits of information.

5. - 12. (Canceled)